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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,277	07/25/2003	Tae W. Kim	OF03P106/US	4246

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,277	KIM, TAE W.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-3,5-9,12-16 and 19* is/are rejected.

7)☒ Claim(s) *4, 10, 11, 17, 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is an official response to the amendment filed on 07 May 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 3, 5, 7- 9, 12, 14-16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shao et al. (US 6,410,394 B1) in view of Stolmeijer et al. (US 5,384,279).

The Shao et al. patent (Shao) discloses a method for fabricating MOS transistors (see figs. 1A,1B, 2A, 2B, 3, and 4 and accompanying text). The method comprises the following steps recited in claim 2: providing a semiconductor substrate 11 (fig. 1A); forming isolation layers 12, wherein the isolation layers is either shallow trench isolation (STI) or field oxide formed by local oxidation of silicon (LOCOS) (fig. 1A and col. 3, lines 19-22); forming a p-well and an n-well in active regions 13 and 15 of the substrate, respectively (col. 3, lines 23-33); forming a sacrificial layer 30 on the semiconductor substrate (fig. 1A and col. 3, lines 39-43); patterning the sacrificial layer to form trenches defining gate electrode forming regions (fig. 1B); conducting ion

implantations for threshold voltage adjustment and punch stop formation on the semiconductor substrate area exposed by the trenches (fig. 2A and col. 4, lines 4-56); forming a gate oxide layer 20 on the surface the substrate under the bottom face of the trenches (fig. 1B); forming a conductive layer on the sacrificial layer so as to completely bury the trench, wherein the conductive layer can be a doped polysilicon layer (col. 4, lines 57-61); polishing the conductive layer until the surface of the sacrificial layer is exposed, so as to form gate electrodes 40 and 50 (fig. 3 and col. 4, lines 64-67); removing the sacrificial layer 30 (col. 5, lines 1-4); forming LDD regions 43 and 42 in the surface of the substrate at both side portions of gate electrodes 40 and 50, respectively (fig. 4); forming spacers 44 on both side walls of gate electrodes 40 and 50 (fig. 4); and forming the source/ drain regions 47 and 46 in the surface of the substrate at both side portions of gate electrodes 40 and 50, respectively, including the spacers 44 (fig. 4).

The implantations for punch stop formation are conducted only under the to-be-gate electrode area.

Boron, phosphorus, and arsenic ions are used for well formation and field stop formation, as recited in claim 7 (col. 4, lines 4-56).

As discussed above, the Shao patent discloses the steps of providing a semiconductor substrate 11; forming isolation layers 12, which is either STI or field oxide; and forming twin wells. However, Shao lacks anticipation in not teaching the following limitations, as recited in claim 2: forming a buffer oxide

layer on the semiconductor substrate; forming the n-well and the p-well by conducting ion implantations through the buffer oxide layer; forming field stop regions, wherein the field stop regions are formed by conducting ion implantations through the buffer oxide, and wherein the implant for field stop formation is made at a sufficient energy to form barriers below the source/ drain junction, as recited in claim 8; and removing the buffer oxide layer.

Again, Stolmeijer discloses a method for fabricating MOS transistors. As previously explained, Stolmeijer discloses the following steps (see the rejection of claim 1 addressed in Section No. 5 of this action): forming a buffer oxide layer 16 on a semiconductor substrate 2 having an isolation layer 7 (fig. 1); and conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer (figs. 1 and 2). The method further comprises a step of removing the buffer oxide layer (fig. 3 and col. 8, lines 49-54). The implant for field stop formation is made at a sufficient energy to form barriers below the source/ drain junctions 22 and 26 (fig. 4 and col. 9, lines 31-34).

Since both the Shao patent and the Stolmeijer patent are from the same field of endeavor, the purpose disclosed by Stolmeijer would have been recognized in the pertinent reference of Shao by one having ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Shao in view of Stolmeijer for reasons as

follows: when the isolation layer 12 (Shao) is field oxide, forming field stop regions, as taught by Stolmeijer, prevents the formation of parasitic transistors below the field oxide regions (Stolmeijer - col. 9, lines 31-34); forming a buffer oxide layer on the substrate, and conducting ion implantations through the buffer oxide layer for formation of the n-well, the p-well, and field stop regions, as taught by Stolmeijer, prevents contamination of the substrate during the implanting step; and removing the buffer oxide layer, as taught by Stolmeijer, provides a clean surface for the subsequent growth of a substantially thin gate oxide layer (Stolmeijer - col. 8, lines 52-54).

While Shao teaches that the sacrificial layer 30 has a thickness ranging from between about 2000 to 4000 A (col. 3, lines 40-43), Shao does not teach that the sacrificial layer is formed to a thickness ranging from between 500 A and 1000 A. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the sacrificial layer to a thickness ranging from between 500 A and 1000 A, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller,105 USPQ 233).

3. Claim 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shao in view of Stolmeijer as applied to claim 2 above, and further in view of Squillace et al. (3,859,222).

While Shao teaches the patterning of sacrificial layer 30, which is preferably composed of silicon nitride, using a reactive ion etching (RIE) process (i.e. dry-etching process) (col. 3, lines 58-62), Shao does not teach that the patterning of the sacrificial layer is implemented via a wet-etching process, as recited in claim 6.

The Squillace et al. patent (Squillace) discloses a method for etching a silicon nitride layer and a silicon oxide layer (figs. 1a-1c and accompanying text). The method comprises a step of patterning a silicon nitride layer 14 using a wet-etching process (fig. 1c and col. 2, line 64 - col. 3, line 7).

Since the Shao patent and the Squillace patent are from the same field of endeavor, the purpose disclosed by Squillace would have been recognized in the pertinent reference of Shao by one having ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Shao and Stolmeijer in view of Squillace, by patterning the sacrificial layer of silicon nitride using a wet-etching process in place of an RIE process, since the wet-etching process creates a smooth slope on the sidewalls of the trench.

Allowable Subject Matter

4. Claim 20 is allowable. Claim 4, 10, 11, 17, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim

and any intervening claims. Shao teaches away from using a sacrificial layer composed of an oxide layer (col. 3, lines 56-67). The trenches are formed in the sacrificial layer 30 using an etchant that has a high selectivity of the sacrificial layer 30 to the gate insulating layer 20. Since the gate insulating layer 20 is composed of oxide, the sacrificial layer 30 cannot be an oxide layer.

Response to Arguments.

5. Applicant's arguments with respect to claims 1, 7, and 8 have been considered but are moot in view of the new ground of rejection.

6. Applicant's arguments regarding the rejection of claims 2, 3, 5, 7, and 8 under 35 USC §103 have been fully considered, but they are not persuasive.

First, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant argues that "Shao '394 cannot disclose or suggest removing a buffer oxide layer before conducting ion implantations for threshold voltage adjustment and punch stop formation, as is recited in amended Claims 1 and 2." The Shao patent is not relied upon for this teaching. As stated in the previous Office action mailed on 13 February 2004, and restated in this action, Stolmeijer discloses the steps of: forming a buffer oxide layer 16 on a semiconductor substrate 2 having an isolation layer 7 (fig. 1); conducting ion

implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer (figs. 1 and 2); and removing the buffer oxide layer (fig. 3 and col. 8, lines 49-54).

Applicant argues that "The silicon oxide layer 16 of Stolmeijer does not correspond to the sacrificial layer recited in amended Claims 1 and 2, because silicon oxide layer 16 is not patterned, it is not removed before conducting ion implantation for punch stop formation, and Stolmeijer does not disclose removal of a different oxide layer prior to its formation". Again, the Stolmeijer patent is relied upon because it teaches the steps of: forming a buffer oxide layer 16 on a semiconductor substrate 2 having an isolation layer 7 (fig. 1); conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer (figs. 1 and 2); and removing the buffer oxide layer (fig. 3 and col. 8, lines 49-54). After the buffer oxide layer 16 is removed, a gate oxide layer 17 is formed on the exposed surface of the substrate (col. 8, lines 49-54). The gate oxide layer 17 of the Stolmeijer patent corresponds to the gate oxide layer 20 in the Shao patent, both of which are formed on an exposed surface of the substrate, as recited in claim 2.

Applicant argues that "Stolmeijer fails to cure the salient deficiencies of Shao '394 with regard to (i) removing a buffer oxide layer before conducting ion implantation for punch stop formation, as is recited in amended Claims 1 and

2. In claims 1 and 2, the buffer oxide layer is removed, not before conducting ion implantation for punch stop formation, but afterwards.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
26 July 2004

Mary Wilczewski
Primary Examiner